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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,405	10/30/2007	Franciscus J. Klosters	NL04 0241 US1	8682

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EXAMINER	
GUYTON, PHILIP A	

ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
01/24/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/590,405	KLOSTERS, FRANCISCUS J.	
	Examiner	Art Unit	
	PHILIP GUYTON	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8,9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20110106*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 6 January 2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 8, 9, and 11-15 are rejected under 35 U.S.C. 103(a) as being obvious over European Patent Pub. No. 0385404 to Nakamura (hereinafter Nakamura) in view of U.S. Patent No. 5,887,129 to Day et al. (hereinafter Day).

With respect to claim 1, Nakamura discloses an electronic circuit arrangement comprising:

a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal (figure 1, clock failure detector 61, 62, 63 and interrupt signal generator 7 and column 2, lines 42-53); and

a processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal (figure 1, diagnosis processor 8 and column 2, lines 49-53 and column 3, lines 27-35), wherein the processor remains dormant in the absence of a clock failure event (column 1, line 57-column 2, line 5).

However, Nakamura does not disclose expressly an asynchronous processor, wherein the asynchronous processor does not receive and is not dependent on any clock signal.

Day teaches an asynchronous processor (figure 2 and column 1, lines 41-55), wherein the asynchronous processor does not receive and is not dependent on any clock signal (column 4, lines 3-6).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Nakamura by including an asynchronous processor, wherein the asynchronous processor does not receive and is not dependent on any clock signal, as taught by Day. A person of ordinary skill in the art would have been motivated to do so because asynchronous processors provide significant power savings when not doing work, according to Day (column 1, lines 26-37 and lines 56-63 and column 1, line 64-column 2, line 9). Accordingly, since the diagnostic processor of Nakamura receives interrupts only when a clock failure occurs, it would have been

obvious to a person of ordinary skill in the art to modify Nakamura with the teachings of Day.

With respect to claim 2, modified Nakamura discloses the asynchronous processor comprises an interrupt input for receiving the error signal (figure 1, signal line 161) and is further arranged to execute software instructions upon reception of the error signal (column 1, line 57-column 2, line 5).

With respect to claim 3, modified Nakamura discloses an integrated circuit comprising an electronic circuit arrangement as claimed in claim 1 (figure 1).

With respect to claim 4, modified Nakamura discloses a bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1 (figure 1).

With respect to claim 6, modified Nakamura discloses a method for bringing an electronic circuit arrangement into a predetermined state, the method comprising:

detecting an absence of a clock signal using a clock fail circuit (column 2, lines 42-48);

generating an error signal in response to the absence of the clock signal (column 2, lines 45-53); and

bringing the electronic circuit arrangement into the predetermined state (column 3, lines 27-35) using an asynchronous processor within the electronic circuit arrangement (Day - figure 2 and column 1, lines 41-55), wherein the asynchronous processor remains dormant in the absence of a clock failure event (column 1, line 57-

column 2, line 5), wherein the asynchronous processor does not receive and is not dependent on any clock signal (Day - column 4, lines 3-6).

With respect to claim 8, modified Nakamura discloses wherein the asynchronous processor does not consume power in the absence of receiving the error signal (Day – column 1, lines 59-60).

With respect to claim 9, modified Nakamura discloses the asynchronous processor executing software instructions upon reception of the error signal (column 1, line 57-column 2, line 5).

With respect to claim 11, modified Nakamura discloses wherein the asynchronous processor does not consume power in the absence of receiving the error signal (Day – column 1, lines 59-60).

With respect to claim 12, modified Nakamura discloses an electronic circuit arrangement comprising:

a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal (column 2, lines 42-53); and

an asynchronous processor (Day - figure 2 and column 1, lines 41-55) arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal (column 3, lines 27-35), wherein the asynchronous processor remains dormant in the absence of a clock failure event (column 1, line 57-column 2, line 5), wherein the asynchronous processor does not consume power in the absence of receiving the error signal (Day – column 1, lines 59-60).

With respect to claim 13, modified Nakamura discloses the asynchronous processor comprises an interrupt input for receiving the error signal (figure 1, signal line 161) and is further arranged to execute software instructions upon reception of the error signal (column 1, line 57-column 2, line 5).

With respect to claim 14, modified Nakamura discloses an integrated circuit comprising an electronic circuit arrangement as claimed in claim 1 (figure 1).

With respect to claim 15, modified Nakamura discloses a bus station comprising an electronic circuit arrangement as claimed in claim 1 (figure 1).

4. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Day, as applied above, and further in view of U.S. Patent No. 6,959,014 to Pohlmeyer et al. (hereinafter Pohlmeyer).

Nakamura and Day do not disclose expressly that the bus station of claim 4 is a bus station for use in a LIN bus system.

However, Pohlmeyer teaches determination of synchronization between transmitters and receivers in a LIN bus system (abstract and column 1, lines 12-27).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Nakamura for use on a LIN bus system, as taught by Pohlmeyer. A person of ordinary skill in the art would have been motivated to do so because it is necessary to retain synchronization between nodes in a LIN bus system, as disclosed by Pohlmeyer (column 1, lines 22-27). Thus, loss of clock, or clock error would be highly detrimental in a LIN bus system (Pohlmeyer - column 2, lines 41-49 and

column 4, lines 1-15). Nakamura teaches a multiprocessor bus system with clock fault determination (figure 1 and abstract), which would have been highly integratable with the LIN bus system of Pohlmeyer, which is also a multiprocessor bus system (column 2, lines 62-64).

Double Patenting

5. Claims 13-16 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 2-5. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP GUYTON whose telephone number is (571) 272-3807. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Philip Guyton/
Primary Examiner, Art Unit 2113